WHAT IS CLAIMED IS:

1. An internal power supply circuit comprising:

a first voltage detector for receiving an external power supply voltage and outputting a first detection signal indicating whether the external power supply voltage is higher than a first voltage;

a first constant voltage generator for generating a first constant voltage from the external power supply voltage;

a second constant voltage generator for generating a second constant voltage from the external power supply voltage, the second constant voltage differing from the first constant voltage, the first constant voltage generator and the second constant voltage generator having identical circuit topologies;

a voltage switch for selecting one of the first constant voltage and the second constant voltage responsive to the first detection signal, and outputting the selected constant voltage as a first reference voltage; and

an internal power supply output unit for generating an internal power supply voltage from the external power supply voltage according to the first reference voltage and outputting the internal power supply voltage.

2. The internal power supply circuit of claim 1, wherein each of the first and second voltage generators comprises an n-channel metal-oxide-semiconductor (NMOS) transistor coupled in series with a pair of resistors.

3. The internal power supply circuit of claim 2, wherein the NMOS transistor has a gate connected to a point between the pair of resistors, and a drain connected to one of the resistors, the constant voltage being obtained from the

drain.

4. The internal power supply circuit of claim 1, wherein the voltage switch comprises:

a buffer amplifier for outputting the first reference voltage;

a first transmission gate for passing the first constant voltage from the first constant voltage generator to the buffer amplifier under control of the first detection signal; and

a second transmission gate for passing the second constant voltage from the second constant voltage generator to the buffer amplifier under complementary control of the first detection signal.

5. The internal power supply circuit of claim 1, wherein the internal power supply output unit comprises:

a differential amplifier having a first input node, a second input node, and an output node;

a first p-channel metal-oxide-semiconductor (PMOS) transistor having a source receiving the first reference voltage from the voltage switch, a gate connected to the first input node of the differential amplifier, and a drain connected to the first input node of the differential amplifier;

a second PMOS transistor having a source connected to the first input node of the differential amplifier, a gate connected to a ground potential, and a drain connected to the ground potential;

a third PMOS transistor having a source receiving the external power supply voltage, a gate connected to the output node of the differential amplifier, and a drain for output of the internal power supply voltage;

a fourth PMOS transistor having a source connected to

the drain of the third PMOS transistor, a gate connected to the second input node of the differential amplifier, and a drain connected to the second input node of the differential amplifier; and

a fifth PMOS transistor having a source connected to the second input node of the differential amplifier, a gate connected to the ground potential, and a drain connected to the ground potential.

6. The internal power supply circuit of claim 5, wherein the differential amplifier comprises:

a sixth PMOS transistor having a source receiving the external power supply voltage, a gate, and a drain connected to the output node of the differential amplifier;

a seventh PMOS transistor having a source receiving the external power supply voltage, a gate connected to the gate of the sixth PMOS transistor, and a drain connected to the gate of the sixth PMOS transistor;

a first NMOS transistor having a source, a gate connected to the first input node of the differential amplifier, and a drain connected to the drain of the sixth PMOS transistor;

a second NMOS transistor having a source, a gate connected to the second input node of the differential amplifier, and a drain connected to the drain of the seventh PMOS transistor; and

a third NMOS transistor having a source connected to the ground potential, a gate receiving a bias voltage, and a drain connected to the source of the first and second NMOS transistors.

7. The internal power supply circuit of claim 1, wherein the first voltage detector comprises:

a reference voltage source for outputting a second

reference voltage;

a constant voltage source for outputting a third constant voltage;

an inverter for outputting the first detection signal;

a first plurality of transistors coupled in series between the external power supply voltage and a ground potential, one of the first plurality of transistors being a PMOS transistor having a gate and a drain, the gate being connected to the reference voltage source; and

a second plurality of transistors coupled in series between the constant voltage source and the ground potential, one of the second plurality of transistors being an NMOS transistor having a gate connected to the drain of the PMOS transistor in the first plurality of transistors, and a drain connected to the inverter.

8. The internal power supply circuit of claim 1, wherein the internal power supply output unit comprises:

a differential amplifier having an output node;

a first transistor having a control terminal connected to the output node of the differential amplifier and an output terminal from which the internal power supply voltage is output;

a second voltage detector for detecting whether the external power supply voltage is higher than a second voltage; and

an auxiliary current supply unit including a second transistor and a third transistor connected in series between the external power supply voltage and the output terminal of the first transistor, the second transistor having a control terminal connected to the output node of the differential amplifier, the third transistor having a control terminal connected to the second voltage detector.

9. The internal power supply circuit of claim 1, further comprising:

a voltage booster for receiving a clock signal and the internal power supply voltage and generating a boosted voltage by using the clock signal to boost the internal power supply voltage;

a second voltage detector for receiving the external power supply voltage and outputting a second detection signal indicating whether the external power supply voltage is higher than a second voltage, the second voltage being lower than the first voltage;

a third voltage detector for receiving the second detection signal and outputting a third detection signal indicating whether the boosted voltage is higher than a third voltage when the second detection signal indicates that the external power supply voltage is higher than the second voltage; and

a clock generator driven by the internal power supply voltage, for generating the clock signal responsive to the third detection signal.

10. The internal power supply circuit of claim 9, wherein the third voltage detector comprises:

a constant voltage source for outputting a third constant voltage;

a reference voltage source for outputting a second reference voltage;

an inverter for outputting the third detection signal;

a first plurality of transistors coupled in series between the boosted voltage and a ground potential, one of the first plurality of transistors being a PMOS transistor having a gate and a drain, the gate being connected to the second voltage detector;

an additional transistor connected in parallel with the

PMOS transistor in the first plurality of transistors, the additional transistor having a gate and a drain, the gate and the drain of the additional transistor being mutually interconnected; and

a second plurality of transistors coupled in series between the constant voltage source and the ground potential, one of the second plurality of transistors being an NMOS transistor having a gate connected to the drain of the PMOS transistor in the first plurality of transistors, and a drain connected to the inverter.

11. An internal power supply circuit for generating an internal power supply voltage from an external power supply voltage that may have different specified voltage levels, the internal power supply circuit comprising:

at least one mode detector for receiving a fixed logic level and thereby generating a mode selection signal indicating one of the different specified voltage levels;

a plurality of voltage detectors for detecting whether the external power supply voltage is higher than different predetermined voltages corresponding to the different specified voltage levels and outputting respective detection signals;

a selector for selecting one of the detection signals according to the mode selection signal;

a first constant voltage generator for generating a first constant voltage from the external power supply voltage;

a second constant voltage generator for generating a second constant voltage from the external power supply voltage, the second constant voltage differing from the first constant voltage, the first constant voltage generator and the second constant voltage generator having identical circuit topologies;

a voltage switch for selecting one of the first constant voltage and the second constant voltage responsive to the detection signal selected by the selector, and outputting the selected constant voltage as a reference voltage; and

an internal power supply output unit for generating an internal power supply voltage from the external power supply voltage according to the reference voltage and outputting the internal power supply voltage.